CLAIMS

I claim:

1. A method of constructing a computing system software on a computer system, wherein said method consisting of:

defining and implementing a plurality of data based on said system's requirements, wherein each said data consists of only two systematic attributes consisting of data value attribute and data timing attribute, consisting only of three types of data:

one or more input data which are imported from input devices of said system; and

one or more middle data which are stored in memory devices of said system; and

one or more output data which are exported by output devices of said system; and

defining and implementing data calculations for each said output data using one or more said middle data and one or more said input data in said system, wherein each said calculation consists of:

one or more mathematic expressions; or

one or more logic expressions; or

one or more experience expressions; or

one or more artificial intelligence expressions; or

derivations of one or more said expressions above; and

executing said implemented calculations to derive both said systematic attributes for each said output data which are development goals of said system software; and

developing safety mechanisms for each said output data to prevent said system software from outputting deviated data if either attribute of said data deviates from their definitions;

wherein developing safety mechanisms for each said output data consists of:

developing reliability defined as that both said data systematic attributes of each output data are matched between their implementations and their definitions, consisting of:

detecting errors consisting only of data value error and data timing error, consisting of: data value error detections, consisting of:

input data value errors detections consisting of checking each said input data implemented value from said input device against said input data transmission protocol; and

middle data value errors detections consisting of checking each said middle data implemented value from said memory devices against said middle data defined value; and

output data value errors detections consisting of checking each said output data implemented value against said output data defined value; and

data timing errors detections, consisting of: input data timing errors detections consisting of checking each said input data available time from said input device against said input data transmission protocol; and

middle data timing errors detections consisting of checking each said middle data available time from said memory device against defined middle data available time; and

output data timing errors detections consisting of checking each said output data implemented said timing attribute against said output data defined time attribute; and

errors reactions, consisting of:

stopping output of said output data if there is any error detected from said output data, or from middle data or input data that are used in said output data's calculation; and

informing said output data's users which are receivers of said output data outside said system about said detected errors; and

recording said detected errors and said errors causes consisting only of:

device defects;

interferences;

development mistakes; and

recovering from said errors if said errors do not exist anymore; and developing availability defined as that neither said output data systematic attributes will be impacted even if there is any error in said data calculations, consisting of developing independent redundant said data calculations; and managing quality of each said output data, consisting of:

verifying if said definitions of said input data and said output data meet said system's requirements; and

verifying if said constructions of both systematic attributes of all said output data satisfy said output data's definitions which are derived from said system's requirements; and

verifying if executions of both systematic attributes of all said output data meet said output data calculation definitions;

wherein said computer system consisting of:

one or more input devices for inputting said input data into said computer system from outside using input transmission protocol; and

one or more output devices for outputting said output data out of said computer system from inside using output transmission protocol; and

one or more memory devices for storing said middle data that are generated during said calculations; and

one or more Arithmetic Logic Unit devices for doing said calculations; and

one or more data transmission links between said devices; and

a management system for managing said devices and said links.

2. The method of claim 1,

wherein each said input data value is defined as value received from said input device; each said input data timing is defined as time when said data is imported from said input device and available to be used by said Arithmetic Logic Unit;

wherein each said middle data value is defined as generated value during said calculation stored in said memory device;

each said middle data timing is defined as time duration reading from said memory device to be available to be used by said Arithmetic Logic Unit;

wherein each said output data value is derived from said implemented calculation;

each said output data timing is calculated as time summary of:

time duration of making all said input and middle data in said output data's calculation to be available to be used by said Arithmetic Logic Unit in said calculation; plus

duration that is used by said Arithmetic Logic Unit to execute said calculation including transmission time that is used by said management system to transmit all said input and middle data in said output data's calculation from their locations to said Arithmetic Logic Unit using said links; plus

duration that said Arithmetic Logic Unit transmits said calculation result data as said output data to said output device; plus

duration that said output device exports said output data from said system.

3. The method of claim 1, wherein implementing said input data consists of:

defining input transmission protocol for each said input data, wherein said protocol defines both systematic attributes of said input data; and

allocating a suitable input device and executing said inputting for each said input data, wherein said device meets said input transmission protocol;

wherein implementing said middle data consists of:

constructing defined generation logic for each said middle data; and

constructing transmission protocol for each said middle data to transmit said middle data between said memory and said Arithmetic Logic Unit, wherein said protocol defines said data two systematic attributes; and

allocating a suitable memory device for each said middle data, wherein said device meets said middle data transmission protocol; and

executing said generation for each said middle data and storing said data into said memory device using said transmission protocol;

wherein implementing said output data and executing said implemented calculations consists of:

constructing defined calculations for each said output data; and

constructing exporting transmission protocol for each said output data, wherein said timing attribute of said protocol is equal or more than said output data's calculated timing attribute; and

transmitting all said input data in said calculation to said Arithmetic Logic Unit using said links by said management system; and

transmitting all said middle data in said calculation to said Arithmetic Logic Unit using said middle data transmission protocol; and

executing said constructed calculation for each said output data; and

allocating a suitable output device for each said output data, wherein said device meets said output data exporting transmission protocol; and

transmitting said output data from said Arithmetic Logic Unit to said output device using said links by said management system for each said output data; and

exporting said output data from said output device for each said output data using said exporting transmission protocol.